

FIG. 1

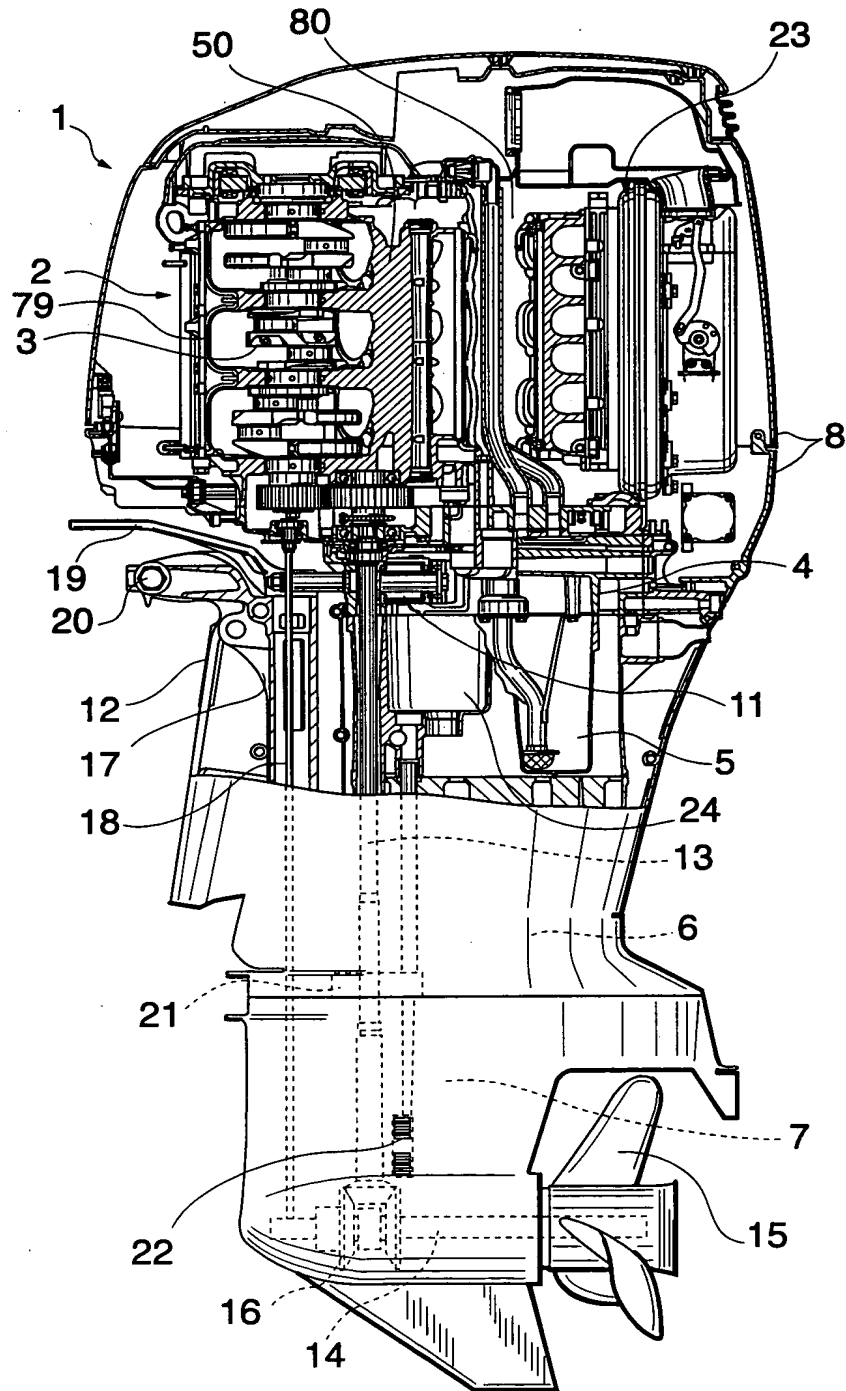


FIG. 2

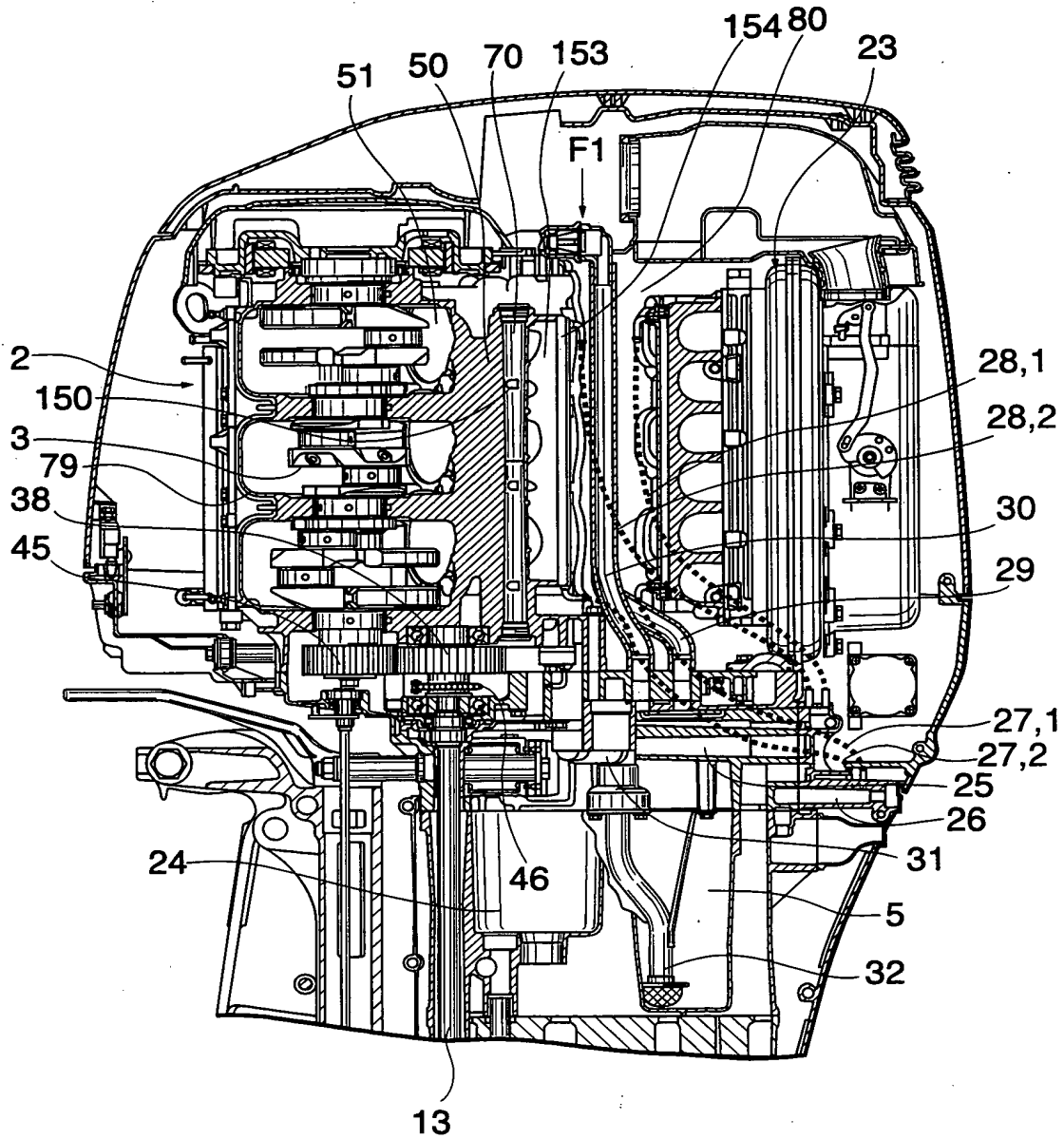


FIG. 3

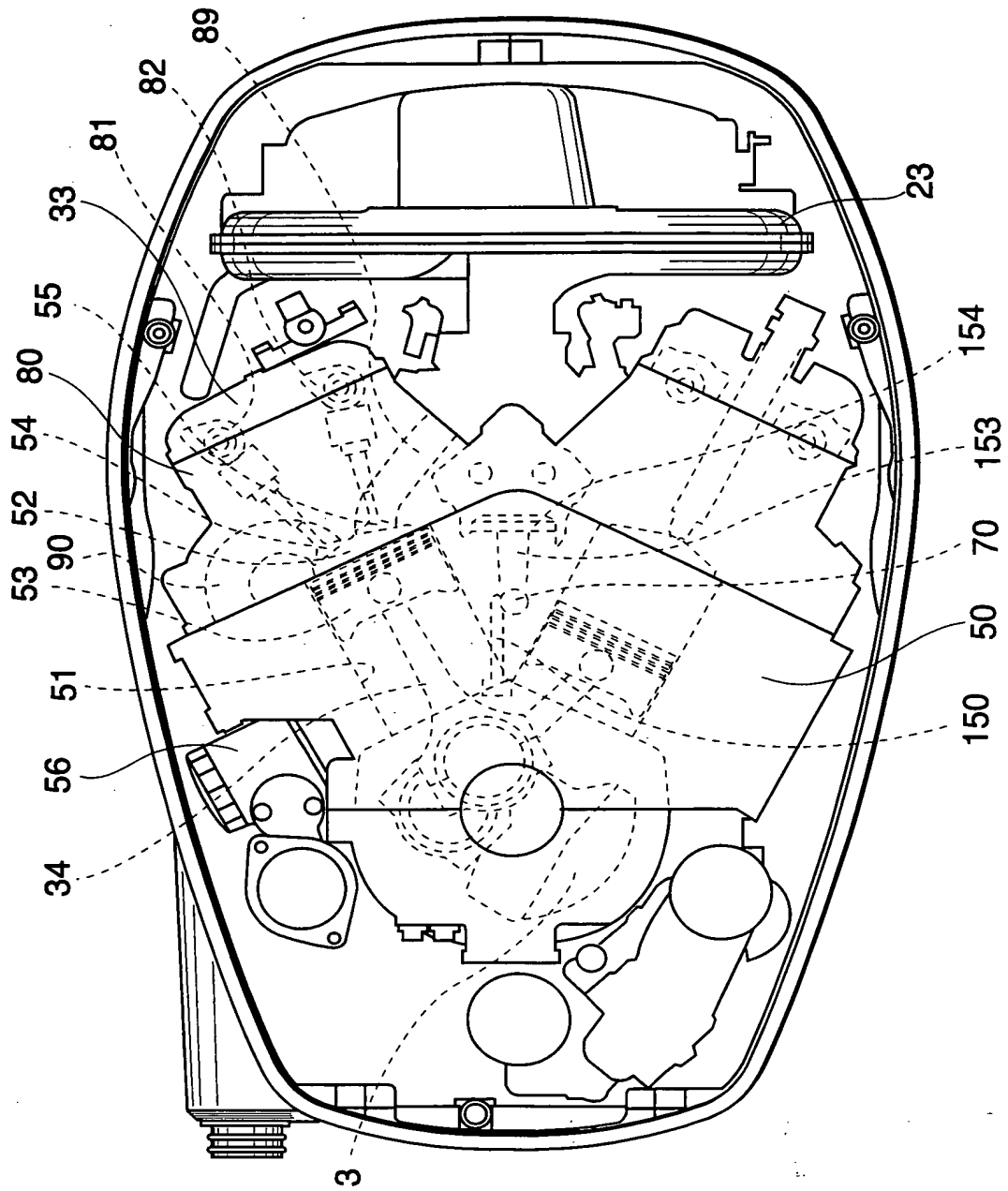


FIG. 4

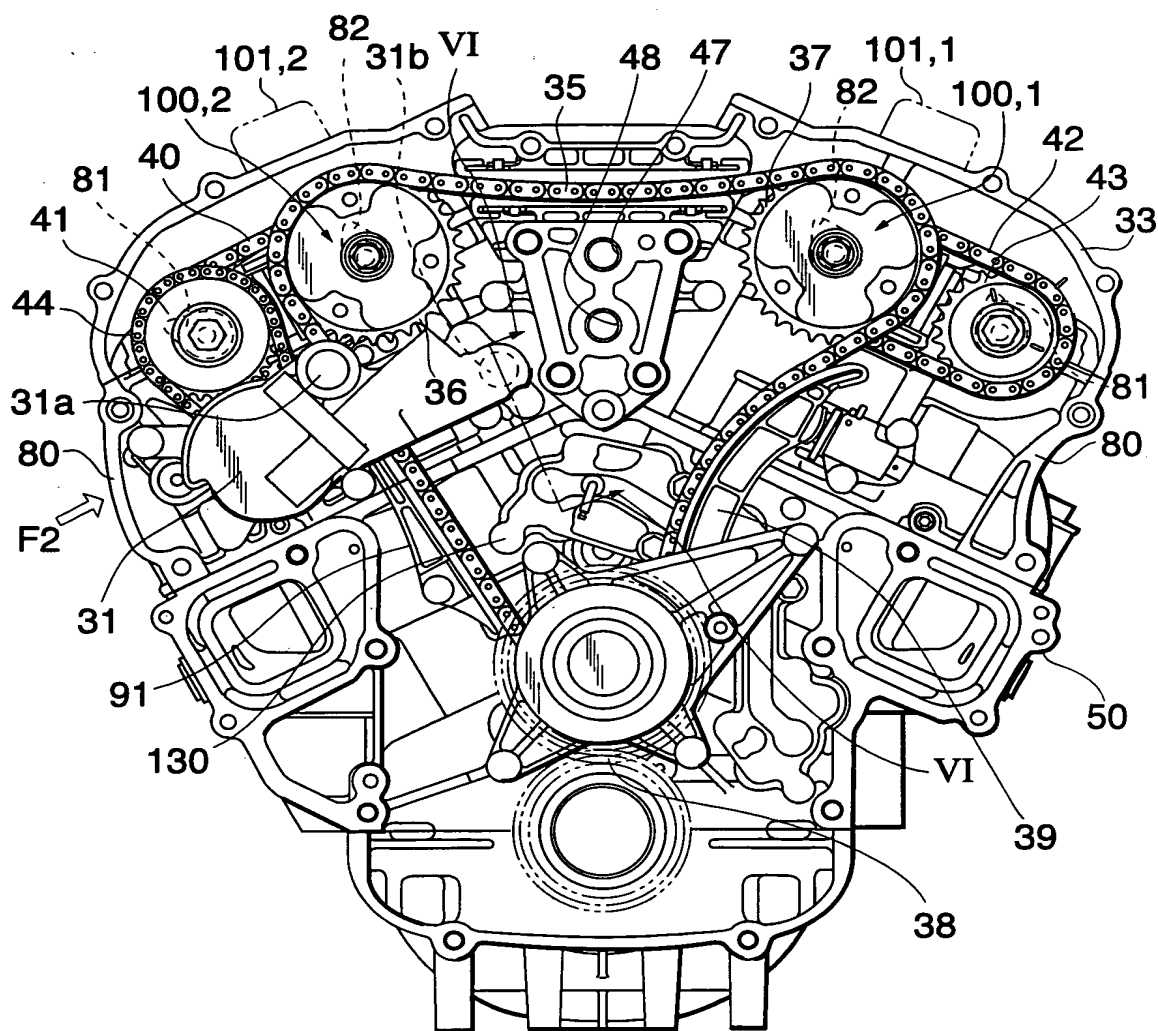
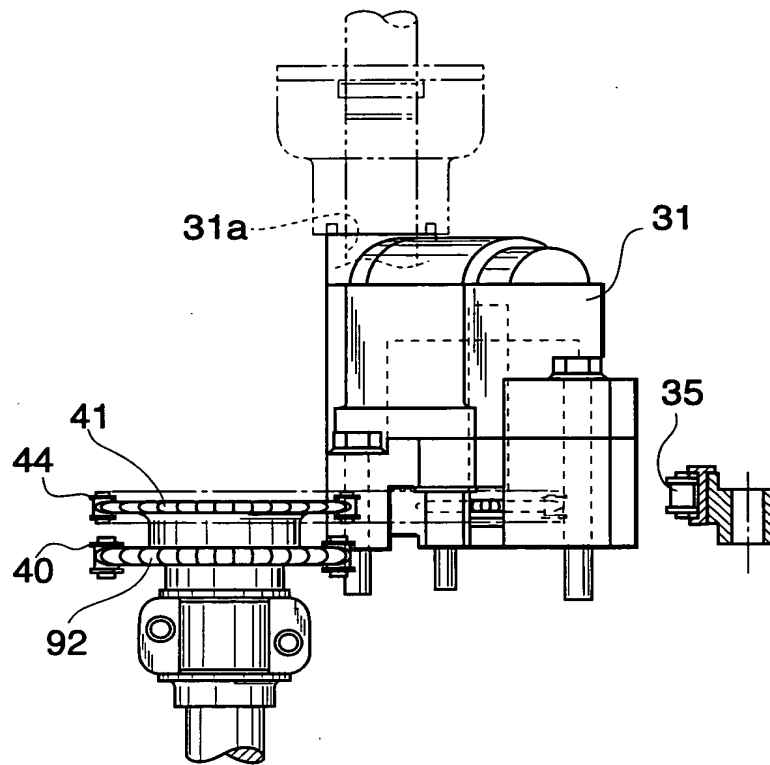


FIG. 5



This cross-sectional diagram illustrates a semiconductor device. A substrate 80 is shown at the bottom, containing a central rectangular region labeled PORT. Above the substrate, there are several layers and structures. On the left side, a layer 31 is shown with a sub-layer 31b. To the right of the PORT region, there is a large rectangular area 50. Above this area, there is a layer 57, which is part of a larger structure 58, 59a. This structure is flanked by two vertical regions labeled PA1 and PA2. At the top, there are additional layers or features labeled 110, 130, and 131b. The entire assembly is supported by a base layer 83, which has sub-regions 83a and 83b.

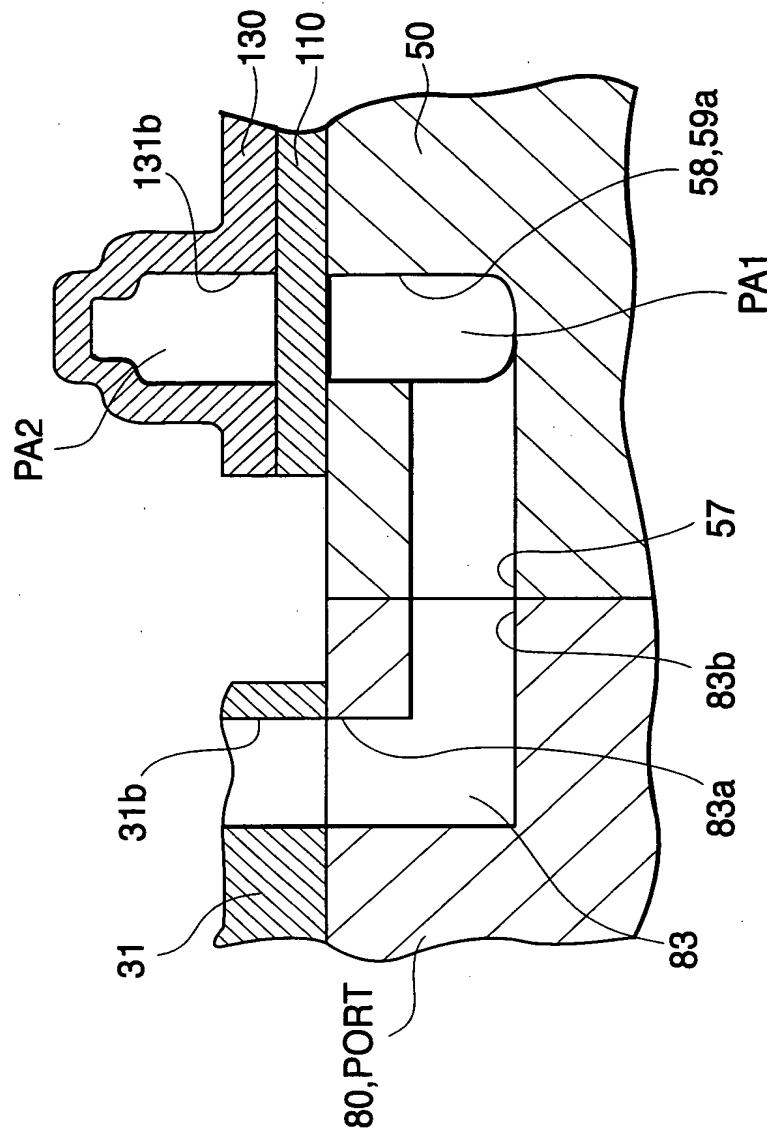


FIG. 7

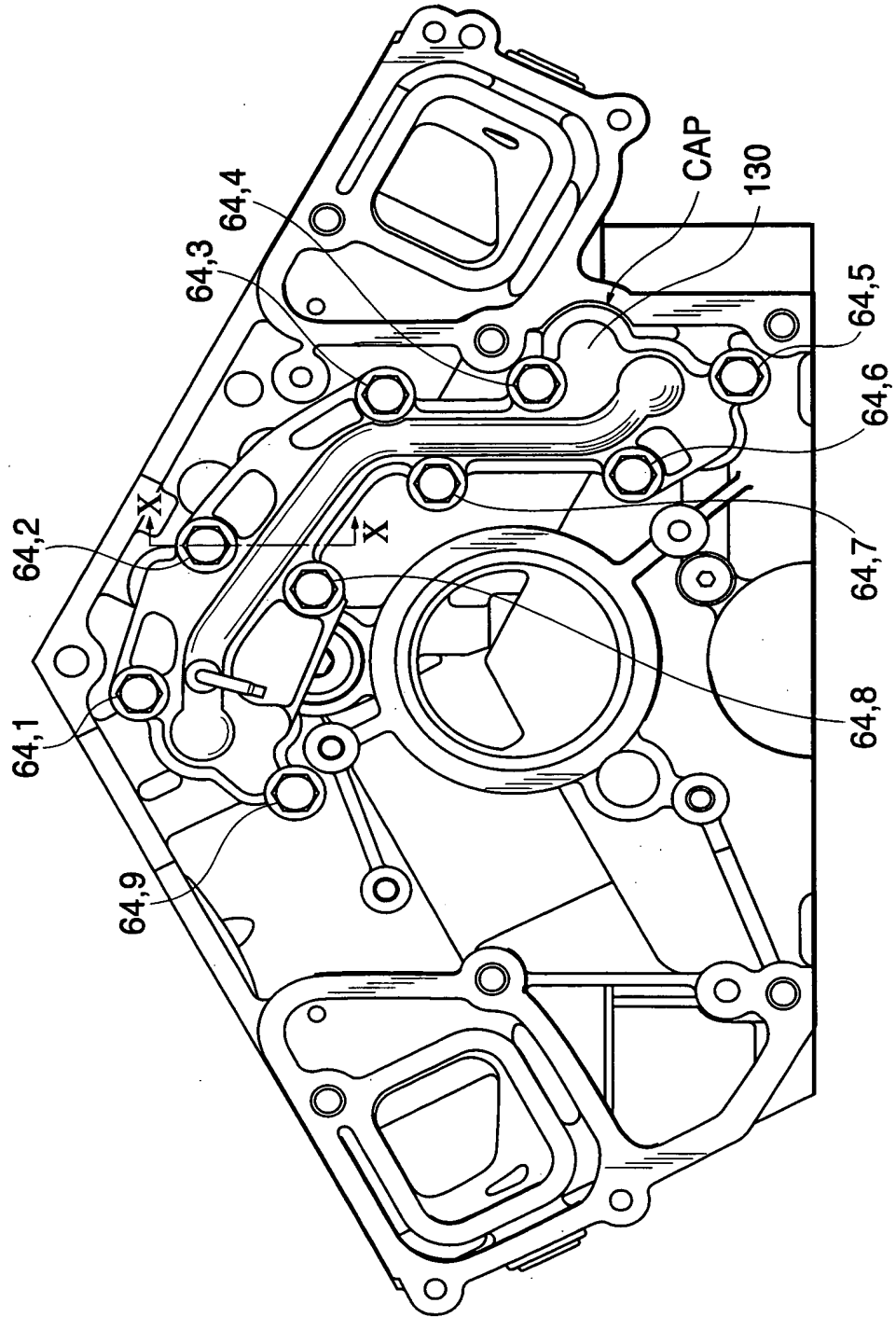
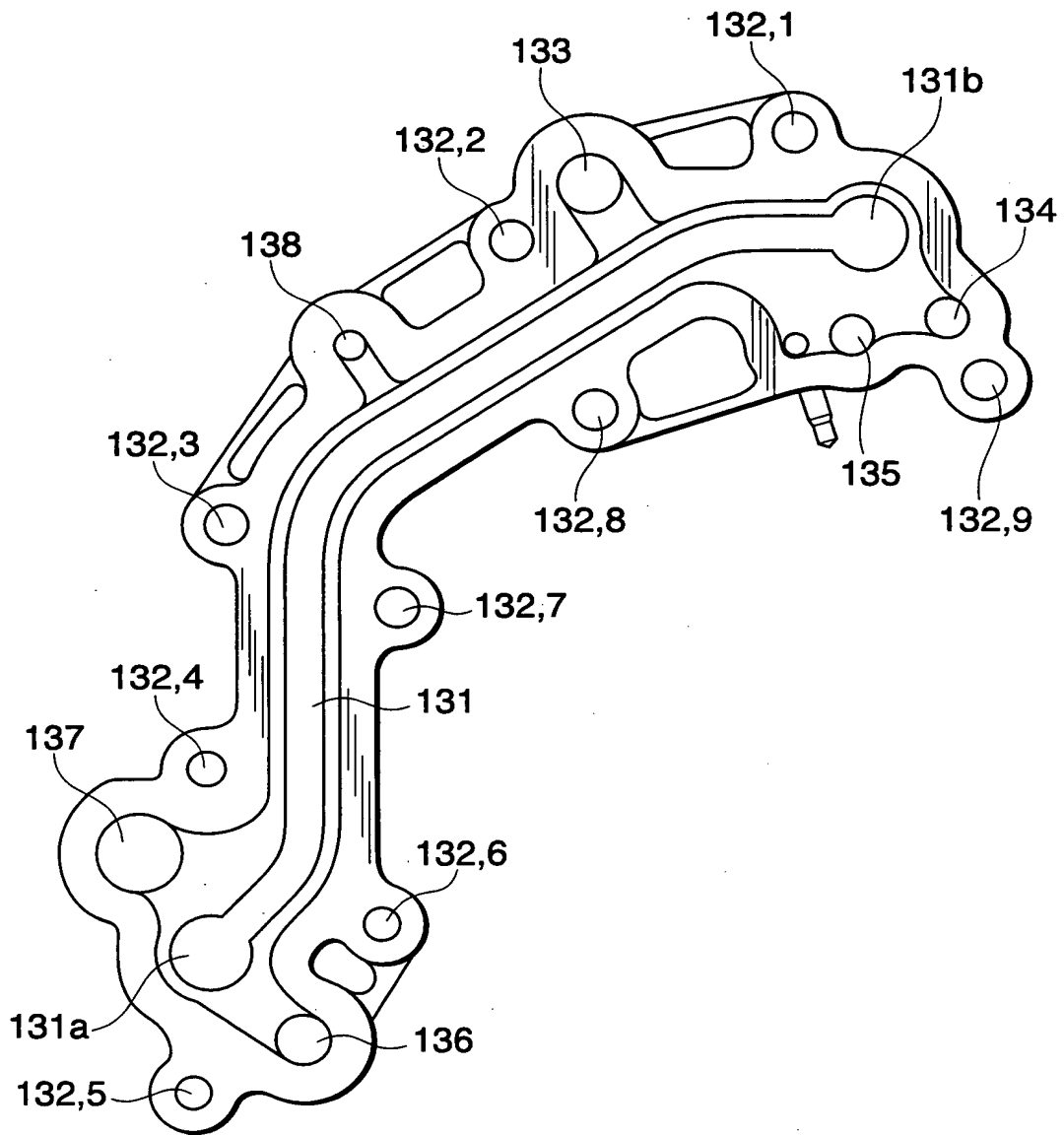
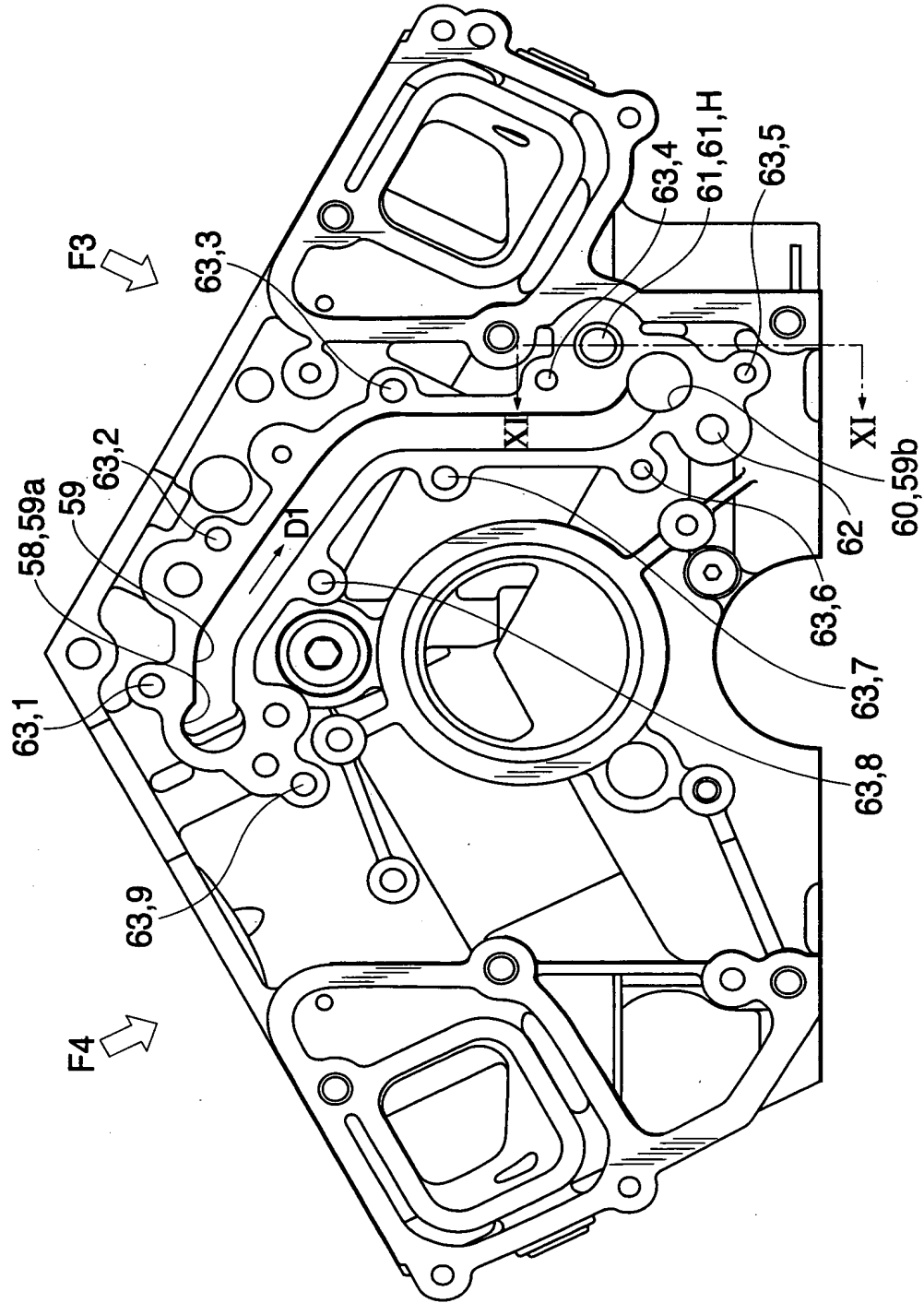


FIG. 8



130

FIG. 9



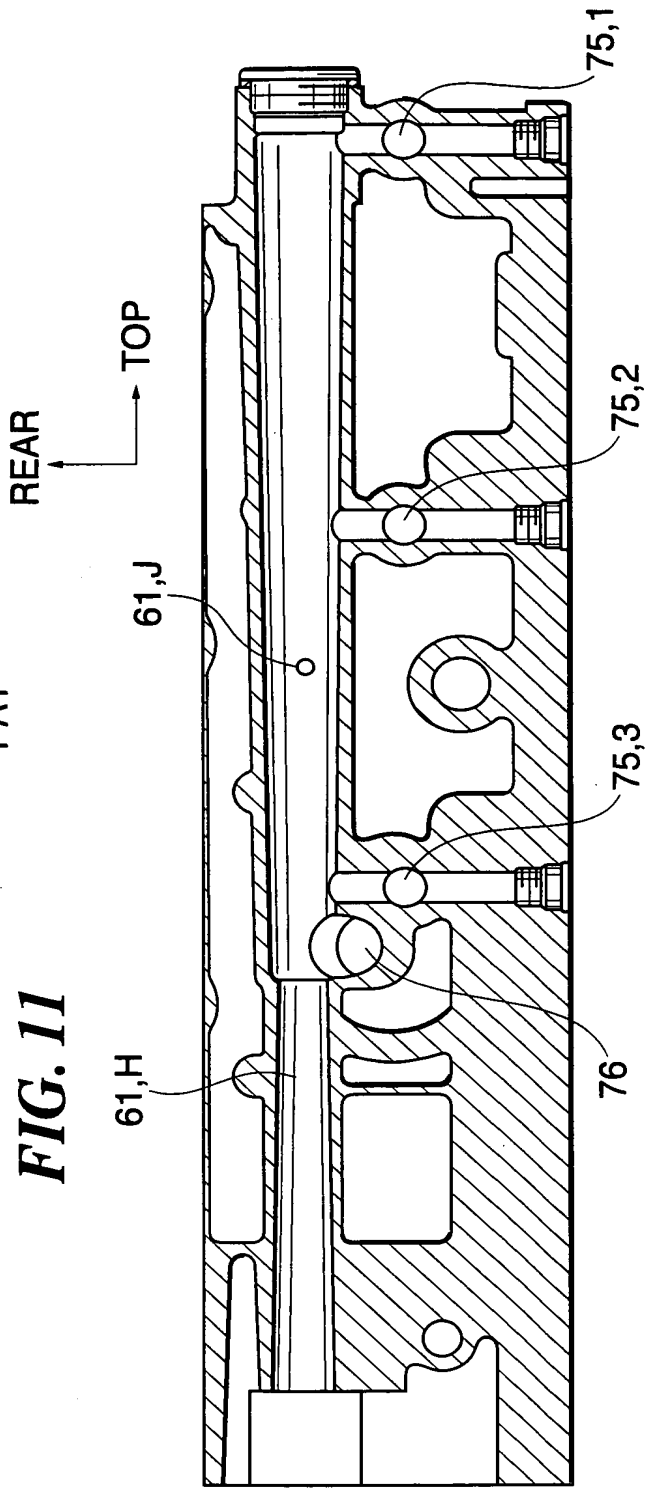
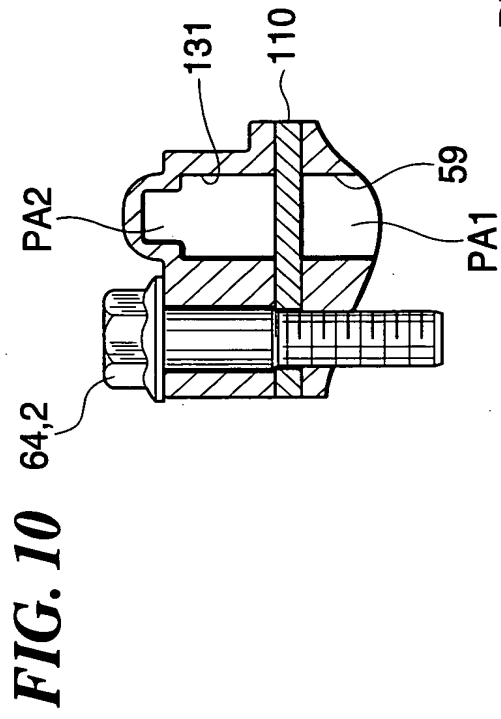


FIG. 12

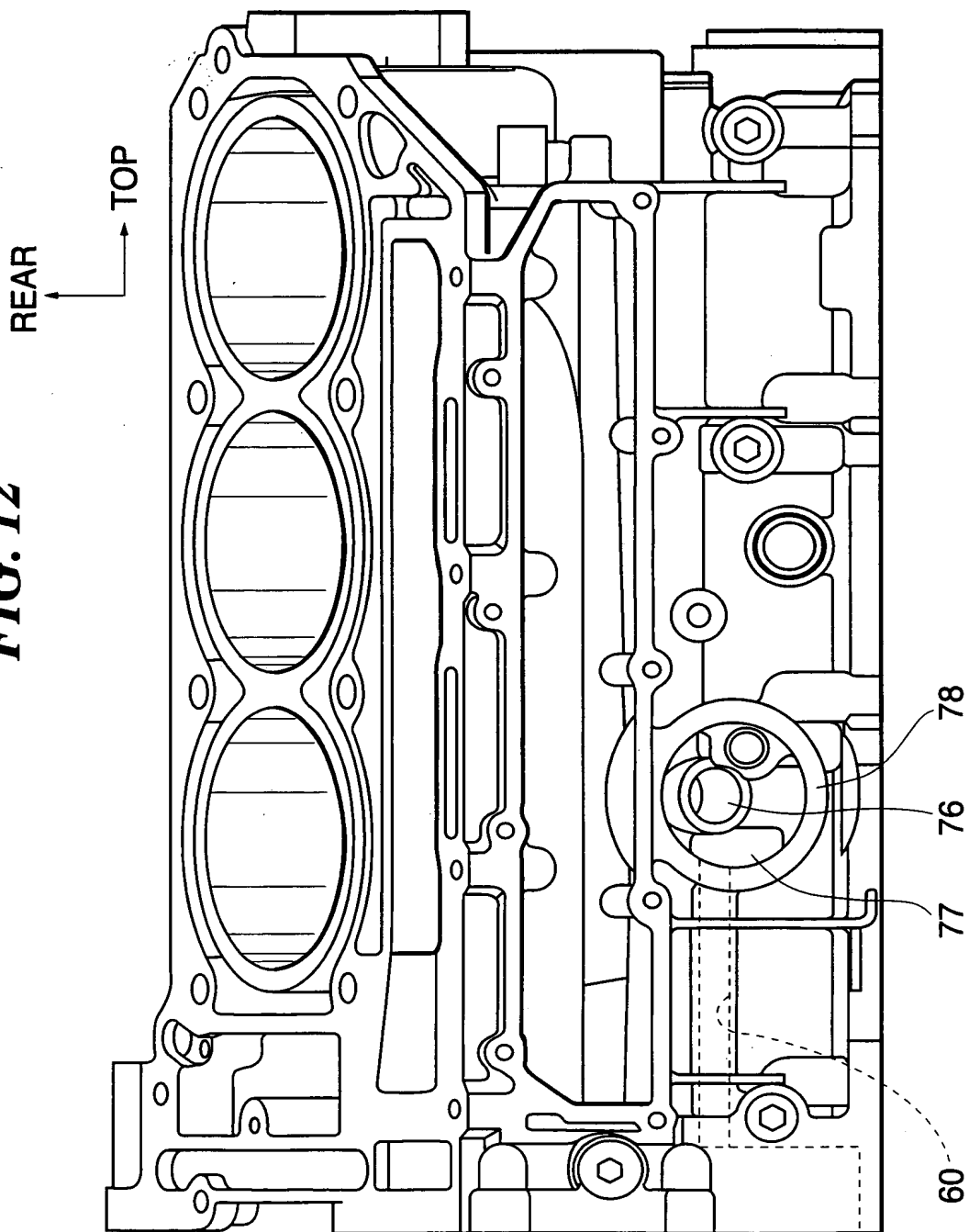


FIG. 13

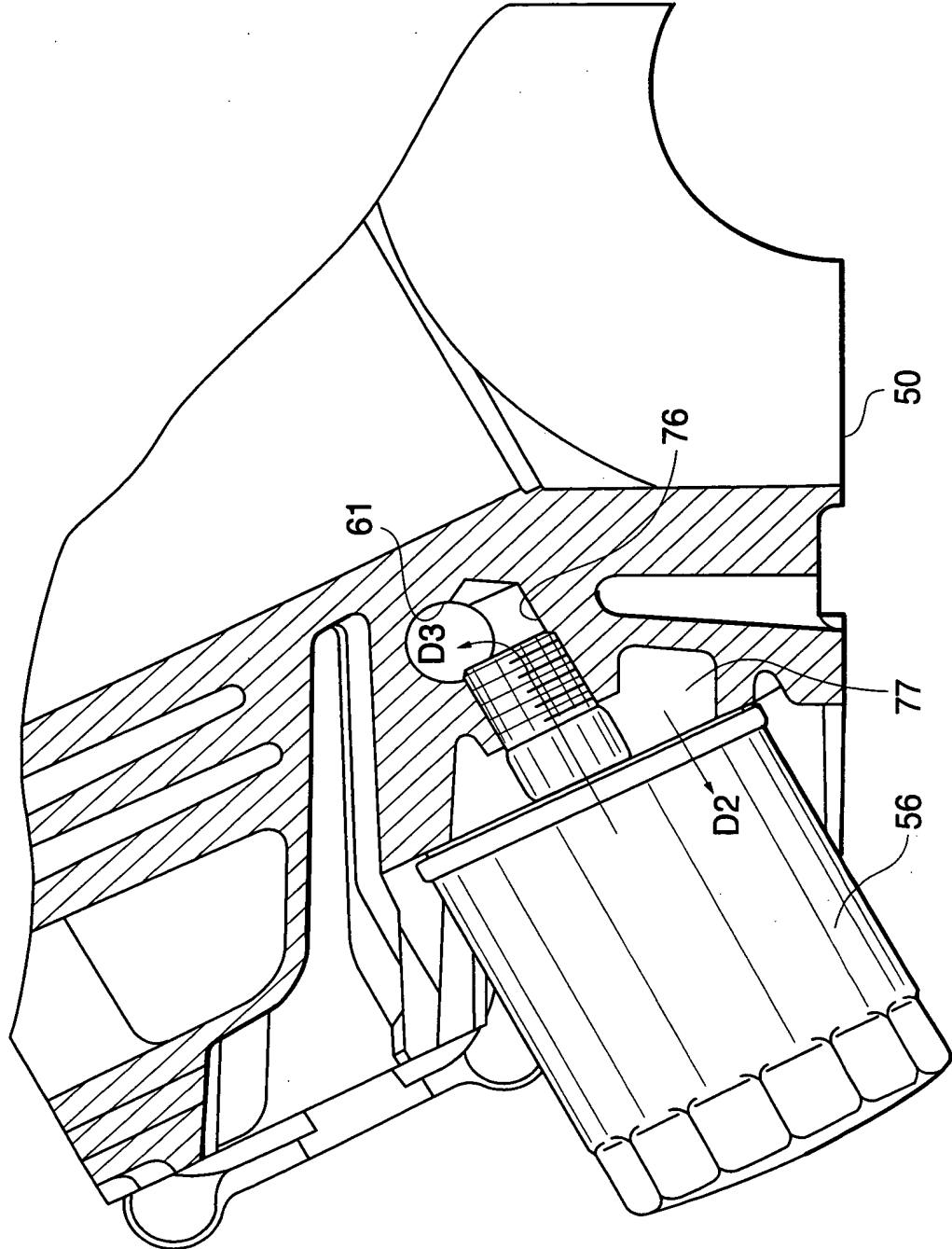


FIG. 14

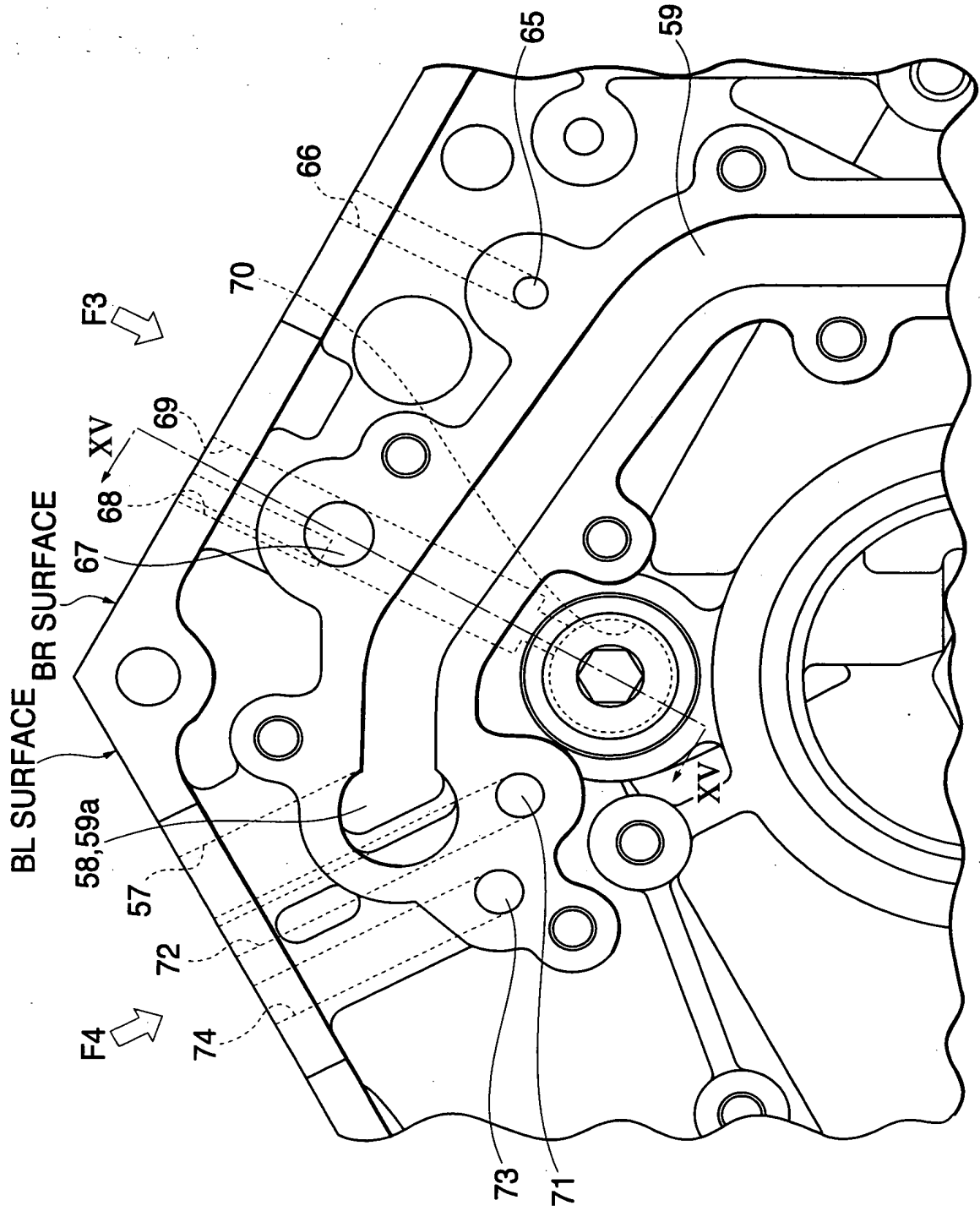


FIG. 15

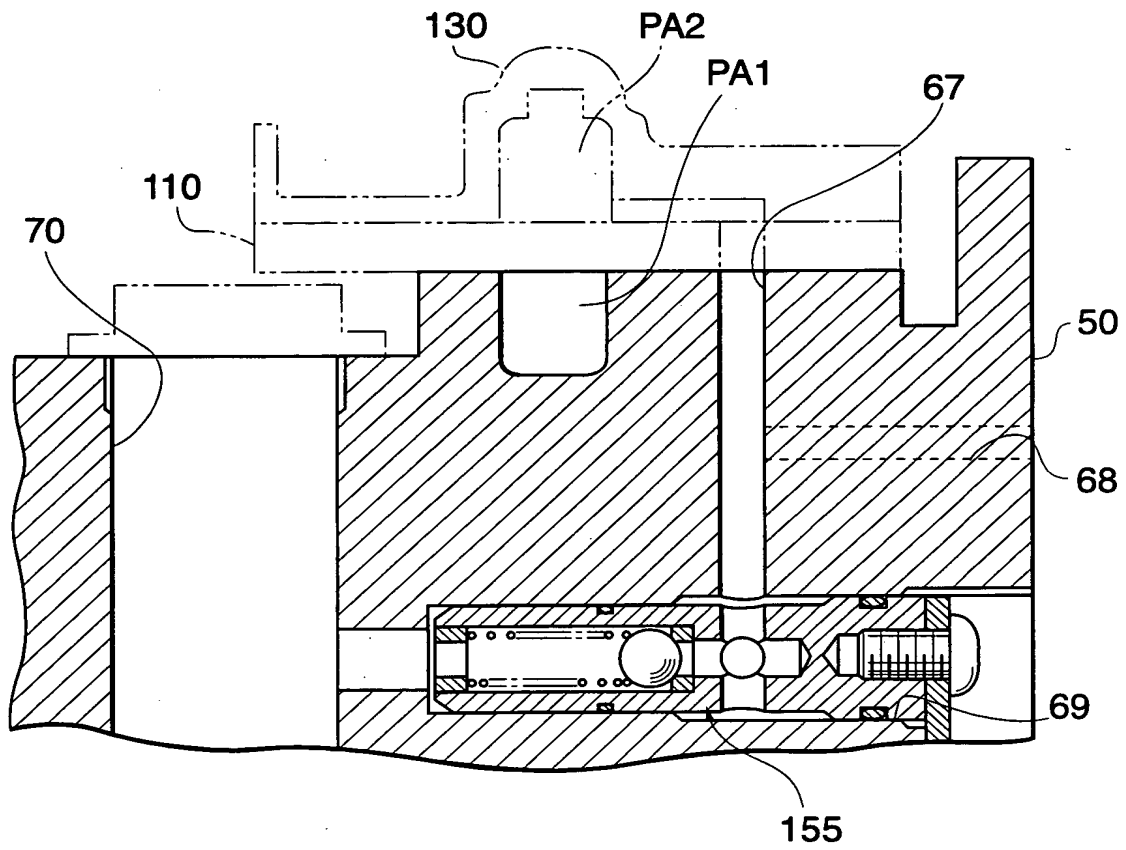


FIG. 16A

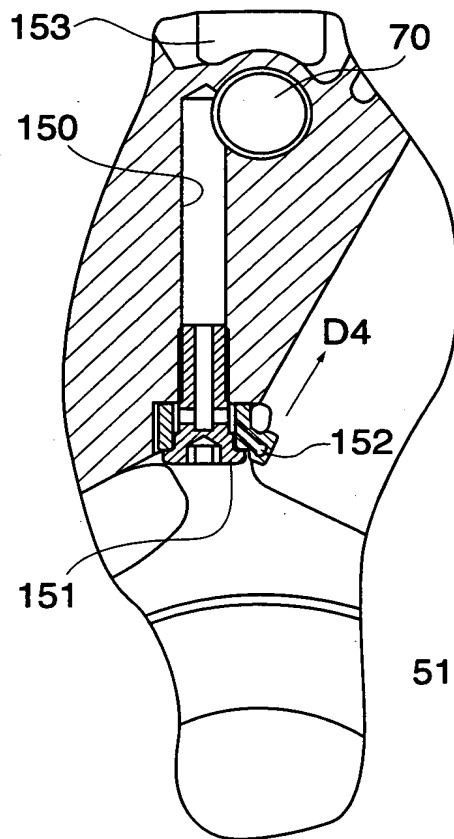


FIG. 16B

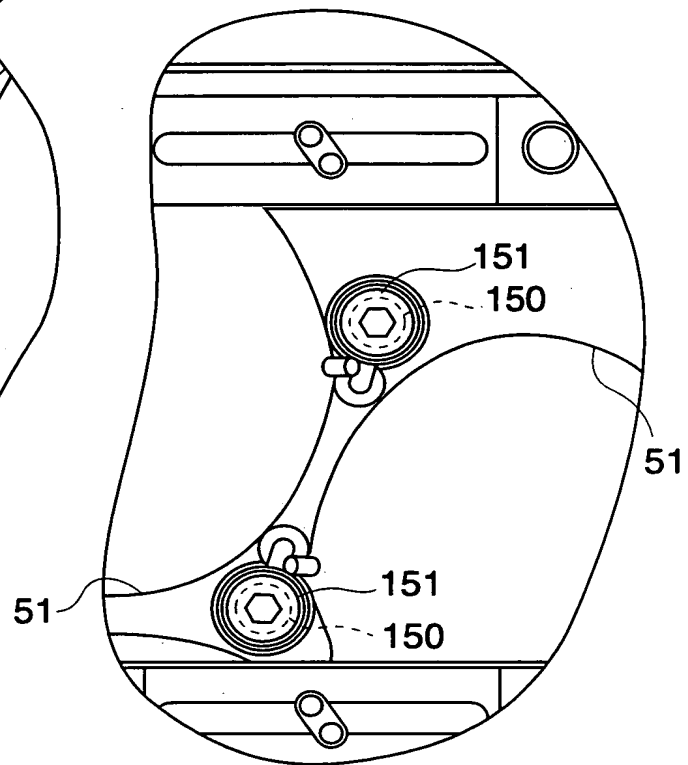


FIG. 17

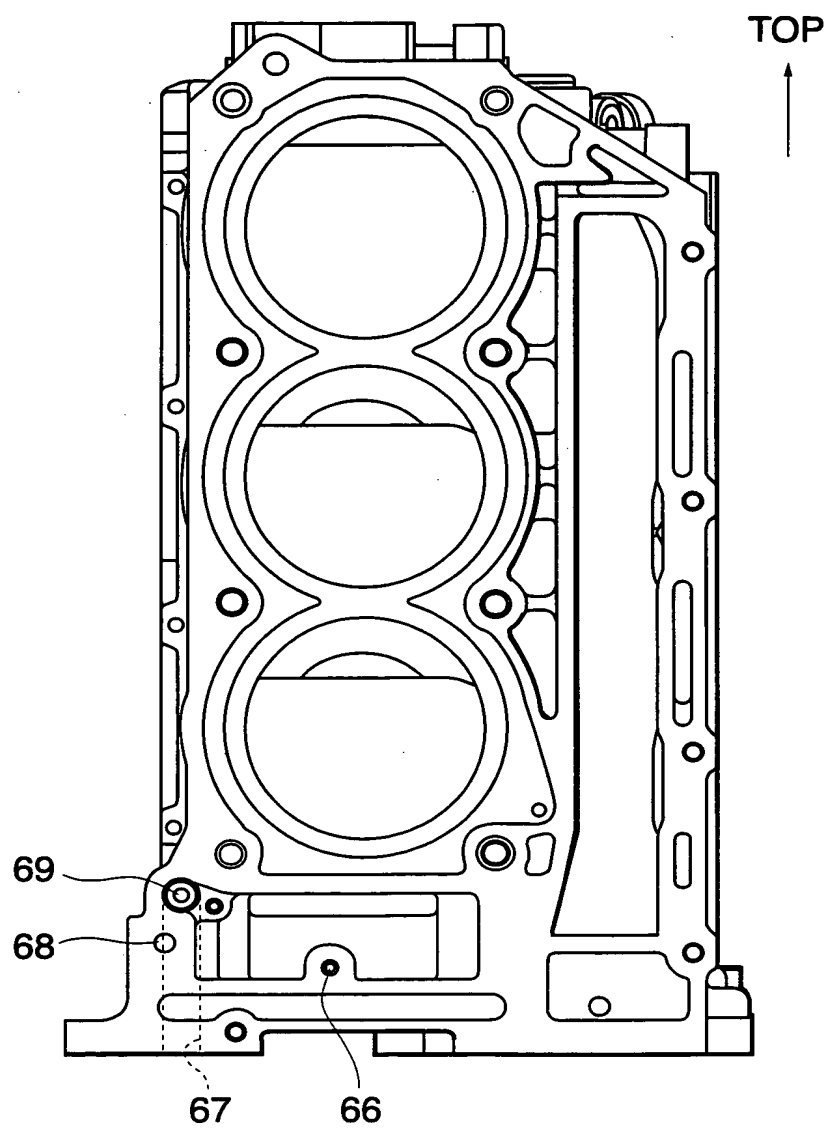


FIG. 18

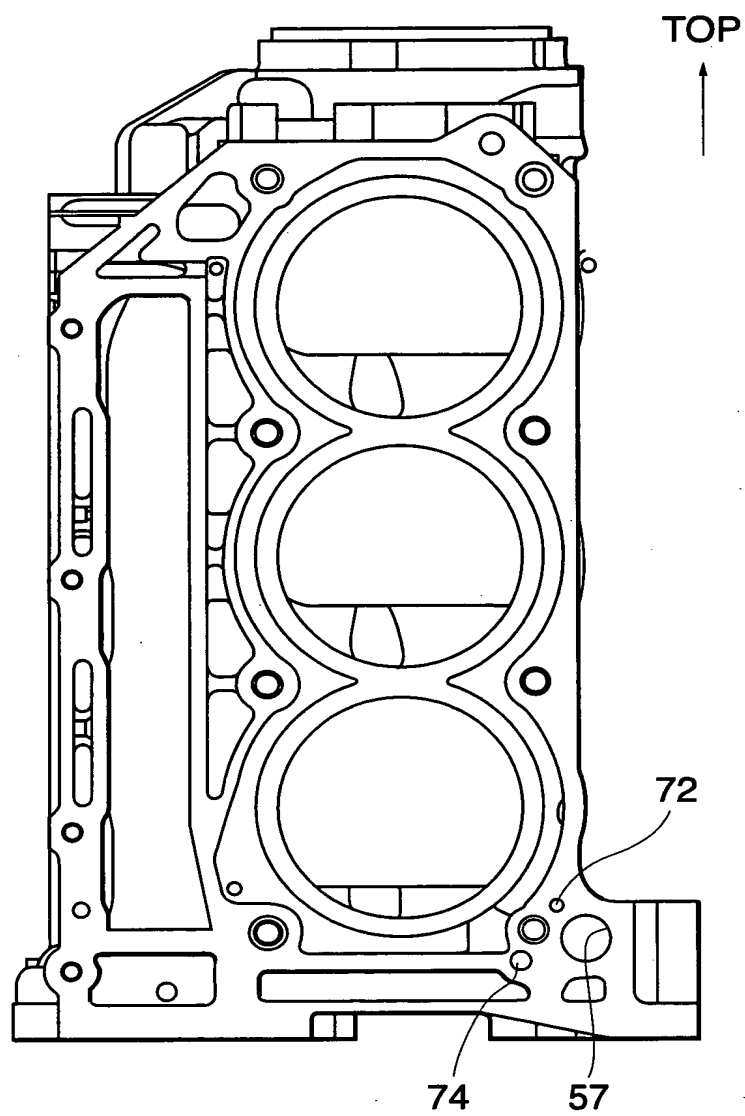


FIG. 19

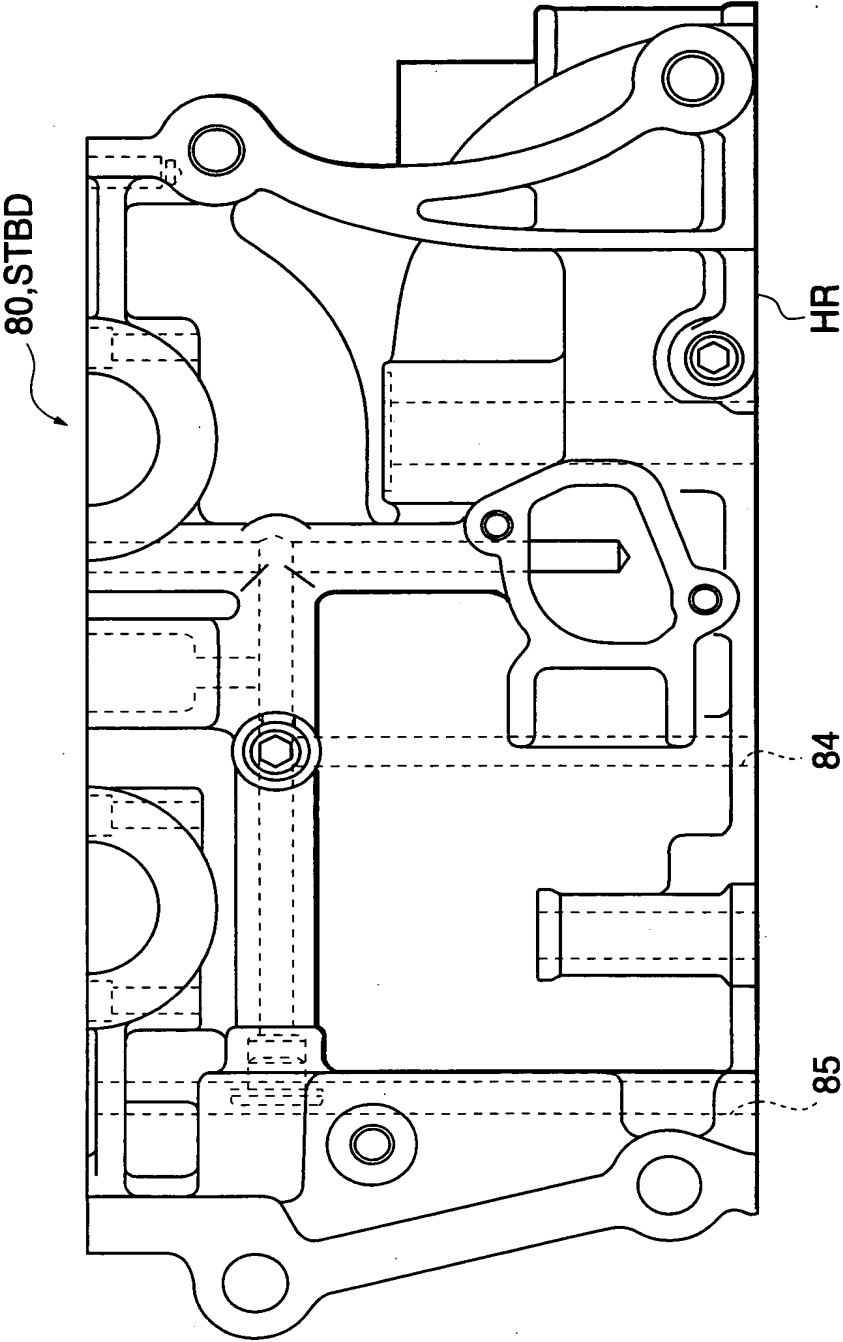


FIG. 20

